

8.5 DC ELECTRICAL SPECIFICATIO

(The electrical specifications in this document are preliminary)

Characteristic
Input High Voltage (except clock)
Input Low Voltage
Clock Input High Voltage
Input Leakage Current (All Input Only Pins) ¹ $V_{in} =$
Three-State (Off State) Input Current @ 2.4 V/0.4 V
Output High Voltage (I_{OH} = Rated Maximum)
Output Low Voltage (I_{OL} = Rated Maximum)
Current Drain ² $T_A = 70^\circ\text{C}$, $V_{CC} = 5.25\text{ V}$, $f = 20\text{ MHz}$
Power Dissipation $f = 20\text{ MHz}$
Input Capacitance ³ All Input-Only Pins All I/O Pins
Load Capacitance ³

1. Not including internal pullup or pulldown

2. Currents listed are with no loading.

3. Capacitance is periodically sampled rather than 100% test

8.6 AC ELECTRICAL SPECIFICATIO

(The electrical specifications in this document are preliminary)

Num	Characteristic
	Frequency of Operation
1	Cycle time
	Crystal Oscillator Start-Up Time
2	EXTAL Pulse Width Low
3	EXTAL Pulse Width High
4,5	EXTAL Rise and Fall Times
1A	External Clock to CLKOUT Skew (Typical)
2A	CLKOUT Pulse Width Low
3A	CLKOUT Pulse Width High

MC68306 USER'S MANUAL ELECTRICAL CHARACTER

This section contains detailed information on the electrical characteristics, and AC timing parameters. Refer to **Section 9 Ordering Information** in the user's manual for specific part numbers, frequency, and temperature ratings.

This device contains protective circuitry to prevent damage to the device from static voltages or electrical fields; however, care should be taken to avoid application of any static voltages to this high-impedance device. The device is enhanced if unused inputs are tied to either GND or VCC).

8.1 MAXIMUM RATINGS

Rating	Symbol	Unit
Supply Voltage ^{1, 2}	V_{CC}	V
Input Voltage ^{1, 2}	V_{in}	V
Operating Temperature Range	T_A	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	$^\circ\text{C}$

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Excess of recommended values affects device reliability while being exposed to electrical extremes.
2. Although sections of the device contain circuitry that is not intended for operation at high voltages or electrical fields, take normal precautions to avoid exposure to rated voltages.

The following ratings define a range of conditions under which the device can operate without being damaged. However, the device should not operate normally while being exposed to these conditions.

8.2 THERMAL CHARACTERISTICS

Characteristic	Symbol
Thermal Resistance—Junction to Case Plastic 132-Pin QFP Plastic 144-Pin Thin QFP	θ_{JC}
Thermal Resistance—Junction to Ambient Plastic 132-Pin QFP Plastic 144-Pin Thin QFP	θ_{JA}

* Estimated

8.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J ,

$$T_J = T_A + (P_D / h_{c,d})$$

where:

T_A = Ambient Temperature, °C

 θ_{JA} = Package Thermal Resistance, $^{\circ}\text{C}/\text{W}$
$$P_D = P_{INT} + P_{I/O}$$
$$P_{INT} = I_C \times V_{CC}, \text{ Watts—Ch}$$

$P_{I/O}$ = Power Dissipation on Input and

For most applications, $P_{I/O} < P_{INT}$ and can

An approximate relationship between P_D and

$$P_D = K \div (T_s)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273)$$

where K is a constant pertaining to the system. K can be determined from equation (3) by measuring P_D (a) at a known value of P_{in} . Using this value of K , the values of F and P_D can be determined from Equations (1) and (2) iteratively for any value of P_{in} .

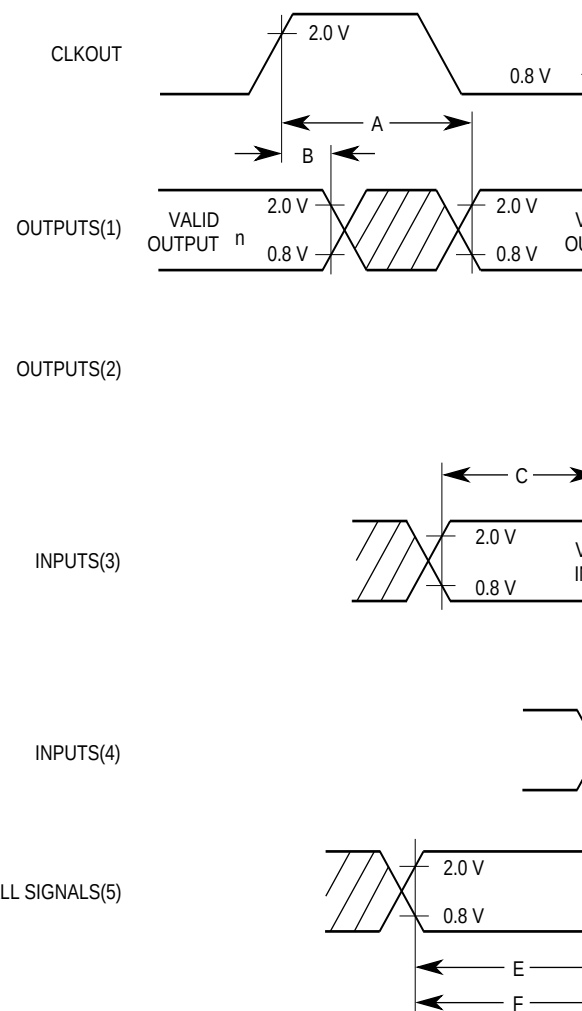
8.4 AC ELECTRICAL SPECIFICATIO

The AC specifications presented consider hold times, and signal skew times. All appropriate edge of the clock and possibly to

The measurement of the AC specific shown in Figure 8-1. To test the par must be driven to the voltage levels specified with minimum and/or maximum measured as shown in Figure 8-1. Input and hold times and are measured as signal-to-signal specifications is also shown.

NO'

The testing levels used to AC specifications do not operation of the device electrical specifications.



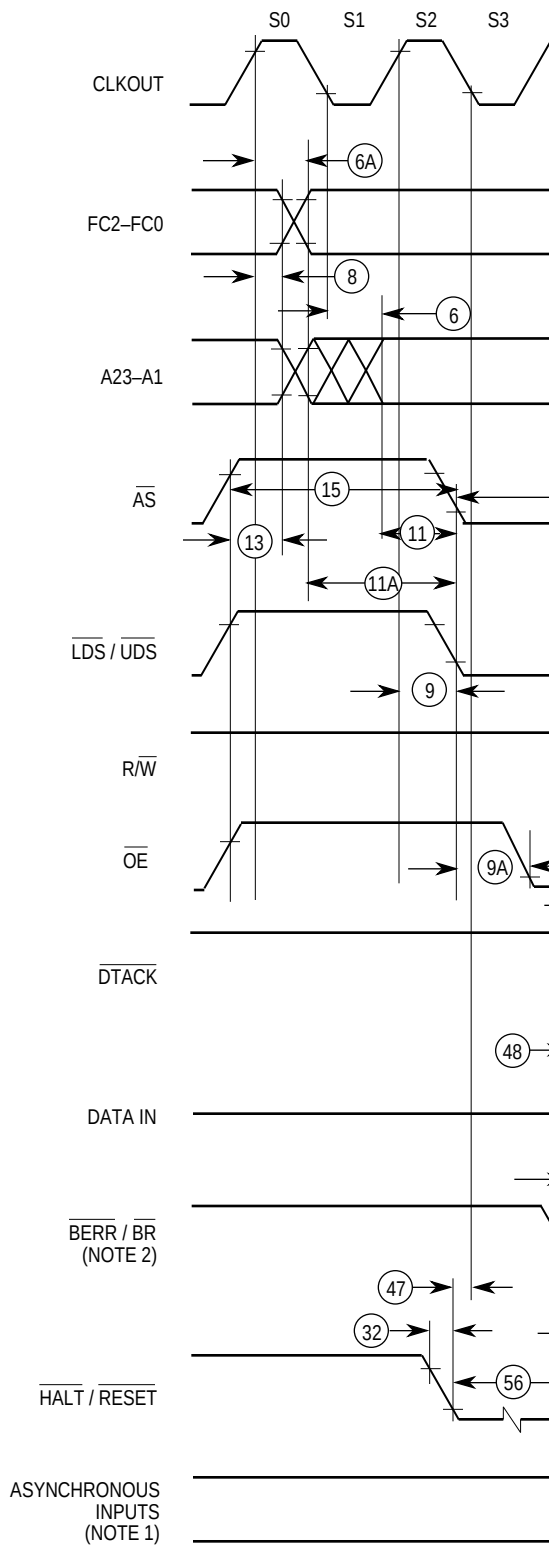
NOTES:

1. This output timing is applicable to all parameters specified
2. This output timing is applicable to all parameters specified
3. This input timing is applicable to all parameters specified r
4. This input timing is applicable to all parameters specified r
5. This timing is applicable to all parameters specified relative

LEGEND:

- A. Maximum output delay specification.
- B. Minimum output hold time.
- C. Minimum input setup time specification.
- D. Minimum input hold time specification.
- E. Signal valid to signal valid specification (maximum or minimum delay).
- F. Signal valid to signal invalid specification (maximum or minimum delay).

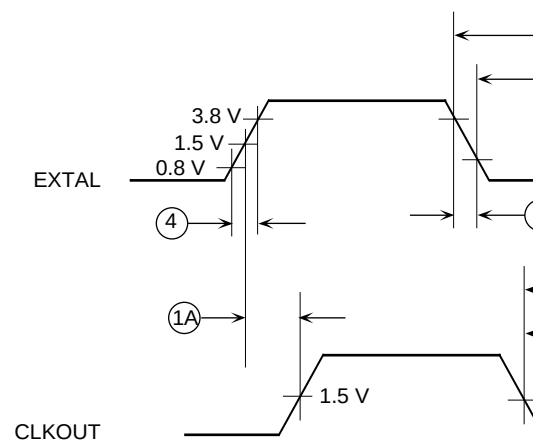
Figure 8-1. Drive Levels



NOTES:

1. Setup time (#47) for asynchronous inputs ($\overline{\text{HALT}}$, $\overline{\text{RI}}$) their recognition at the next falling edge of the clock
2. $\overline{\text{BR}}$ need fall at this time only to ensure being recogni

Figure 8-3. Read



NOTE: Timing measurements are referen
voltage of 3.8 V, unless otherwise
should start outside and pass thr
between 0.8 V and 3.8 V.

Figure 8-2. C

8.7 AC ELECTRICAL SPECIFICATI CYCLES

(The electrical specifications in this docum

Num	Characteristic
6	CLKOUT Low to Address Valid (Row Address for Cycle)
6A	CLKOUT High to FC Valid
7	CLKOUT High to Data Bus High Impedance (Ma
8	CLKOUT High to Address, FC Invalid (Minimum)
9 ¹	CLKOUT High to AS, LDS, UDS Asserted
9A	UDS, LDS Asserted to OE, UW, LW Asserted
11 ²	Address Valid to AS, LDS, UDS Asserted (Read) Asserted (Write)
11A ²	FC Valid to AS, LDS, UDS Asserted (Read)/ AS, (Write)
12 ¹	CLKOUT Low to AS, LDS, UDS Negated
12A	UDS, LDS Negated to OE, UW, LW Negated
13 ²	AS, LDS, UDS Negated to Address, FC Invalid
14 ²	AS (and LDS, UDS Read) Width Asserted
14A ²	LDS, UDS, Width Asserted (Write)
15 ²	AS, LDS, UDS Width Negated
16	CLKOUT High to Control Bus High Impedance
17 ²	AS, LDS, UDS Negated to R/W Invalid
18 ¹	CLKOUT High to R/W High (Read)
20 ¹	CLKOUT High to R/W Low (Write)

8.7 AC ELECTRICAL SPECIFICATIO CYCLES (Continued)

designer wishes to decode more chip selects than the external decode.

Num	Characteristic
20A ⁶	AS Asserted to R/W Low (Write)
21 ²	Address Valid to R/W Low (Write)
21A ²	FC Valid to R/W Low (Write)
22 ²	R/W Low to LDS, UDS Asserted (Write)
23	CLKOUT Low to Data-Out Valid (Write)
25 ²	AS, LDS, UDS Negated to Data-Out Invalid (Write)
26 ²	Data-Out Valid to LDS, UDS Asserted (Write)
27 ⁵	Data-In Valid to CLKOUT Low (Setup Time on Re
28 ²	AS, LDS, UDS Negated to DTACK Negated (Asyn Hold)
29	AS, LDS, UDS Negated to Data-In Invalid (Hold Ti Read)
29A	AS, LDS, UDS Negated to Data-In High Impedanc
30	AS, LDS, UDS Negated to BERR Negated
31 ^{2,5}	DTACK Asserted to Data-In Valid (Setup Time)
32	HALT and RESET Input Transition Time
47 ⁵	Asynchronous Input Setup Time
48 ³	BERR Asserted to DTACK Asserted
53	Data-Out Hold from CLKOUT High
55	R/W Asserted to Data Bus Impedance Change
56 ⁴	HALT/RESET Pulse Width

NOTES:

1. For a loading capacitance of less than or equal to 5 maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both DTACK and BERR, #48 n is an asynchronous input using the asynchronous ir
4. For power-up, the MC68306 must be held in the res on-chip circuitry. After the system is powered up, #56 refers reset the controller.
5. If the asynchronous input setup time (#47) requirem asserted to data setup time (#31) requirement can be ignored. The d setup time (#27) for the following clock cycle.
6. When AS and R/W are equally loaded ($\pm 20\%$), subt columns.
7. The processor will negate BG and begin driving the BR before asserting BGACK.
8. The minimum value must be met to guarantee prop BG may be reasserted.
9. AS is always asserted, regardless of whether it is m

8.9 AC ELECTRICAL SPECIFICATIO

electrical specifications in this document are preliminary. S

Num	Characteristic
7	CLKOUT High to Address, Data Bus High Impeda
16	CLKOUT High to Control Bus High Impedance
33	CLKOUT High to BG Asserted
34	CLKOUT High to BG Negated
35	BR Asserted to BG Asserted
36	BR Negated to BG Negated
37	BGACK Asserted to BG Negated
37A ²	BGACK Asserted to BR Negated
38	BG Asserted to Control, Address, Data Bus High Negated)
39	BG Width Negated
47	Asynchronous Input Setup Time
57	BGACK Negated to Bus Driven
58	BR Negated to Bus Driven

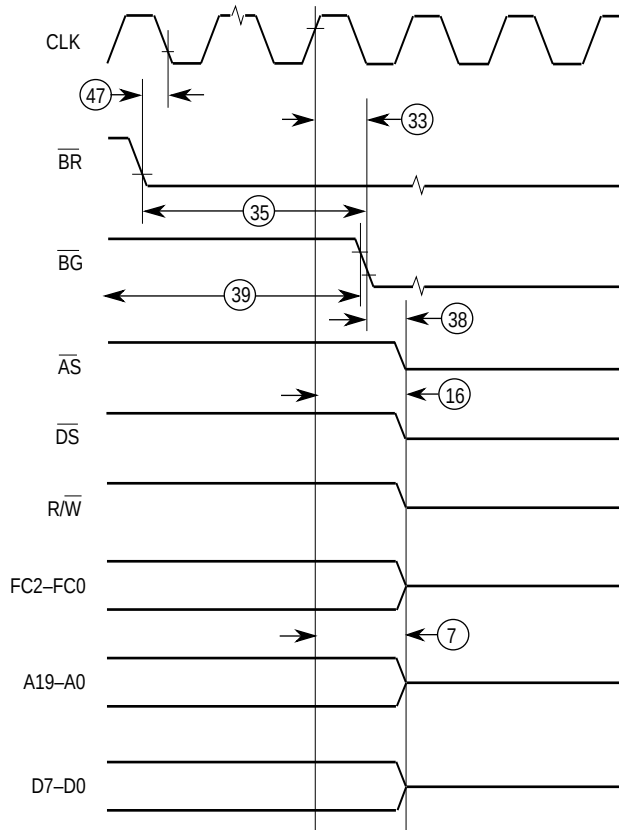
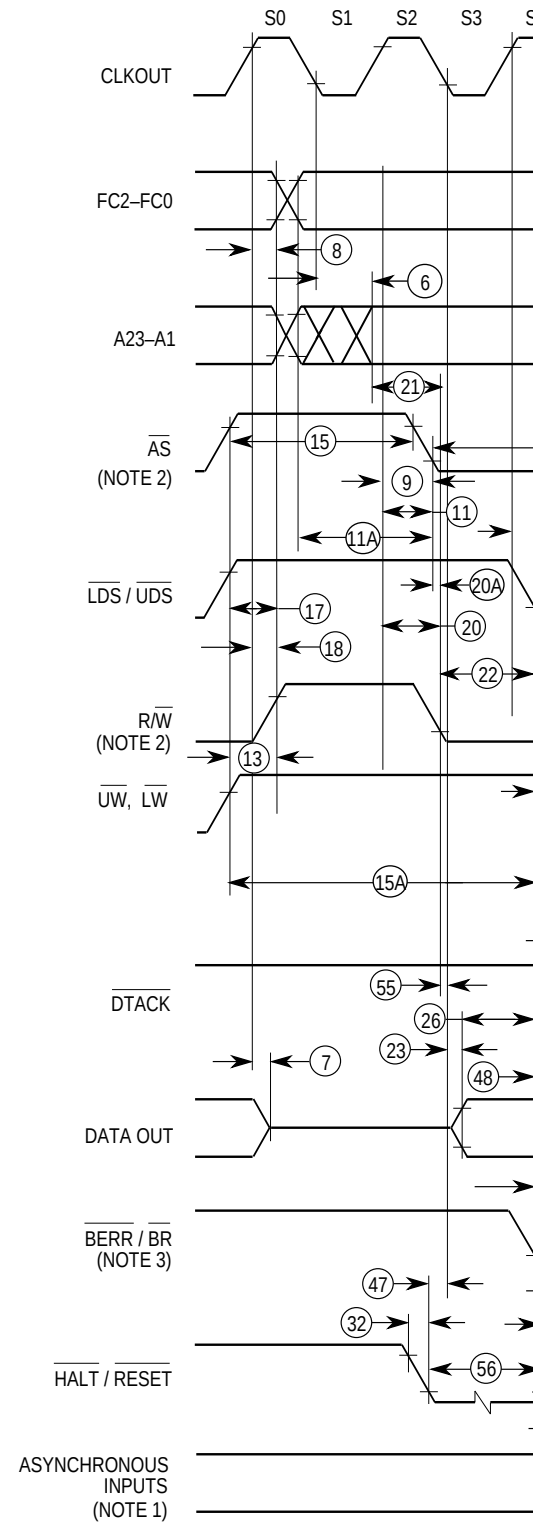


Figure 8-6. Bus A



NOTES:

1. Setup time (#47) for asynchronous inputs (HALT, RESET, BERR, BR) to ensure their recognition at the next falling edge of the clock.
2. Because of loading variations, R/W may be valid at the falling edge of S2 (specification #20A).
3. BR need fall at this time only to ensure being recognized.

Figure 8-4. Writing to Memory

8.8 AC ELECTRICAL SPECIFICATIC INTERRUPT ACKNOWLEDGE (The ele preliminary.)

Num	Characteristic
61	Address Valid to CS $\approx$ Asserted (Read or Write)
61A	FC Valid to CS $\approx$ Asserted (Read or Write)
62	AS $\vee$ DS to CS $\approx$
63	AS $\vee$ R/W to CS $\approx$
64	CS $\approx$ Width Asserted
65	CS $\approx$ Negated to FC, Address Invalid
66	CS $\approx$ Negated to R/W Invalid
67	Data-Out Valid to CS $\approx$ Negated (Write)
68	CS $\approx$ Negated to Data-Out Invalid (Write)
69	CS $\approx$ Negated to Data-In High Impedance
70	CLKOUT High to IACK $\approx$ Asserted
70A	LDS High to IACK $\approx$ Negated

$\vee$ = Boolean OR

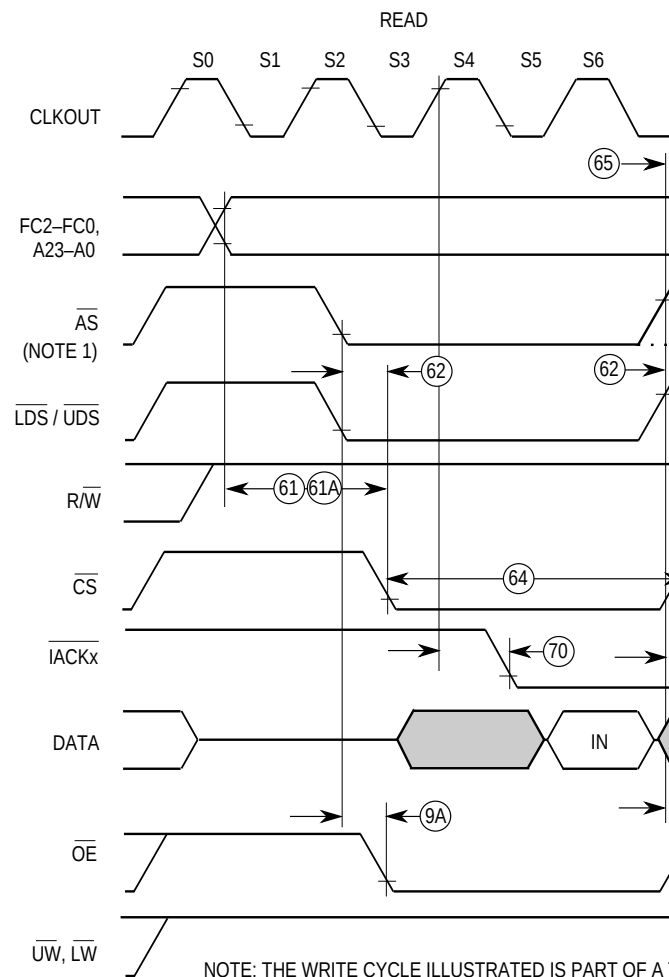
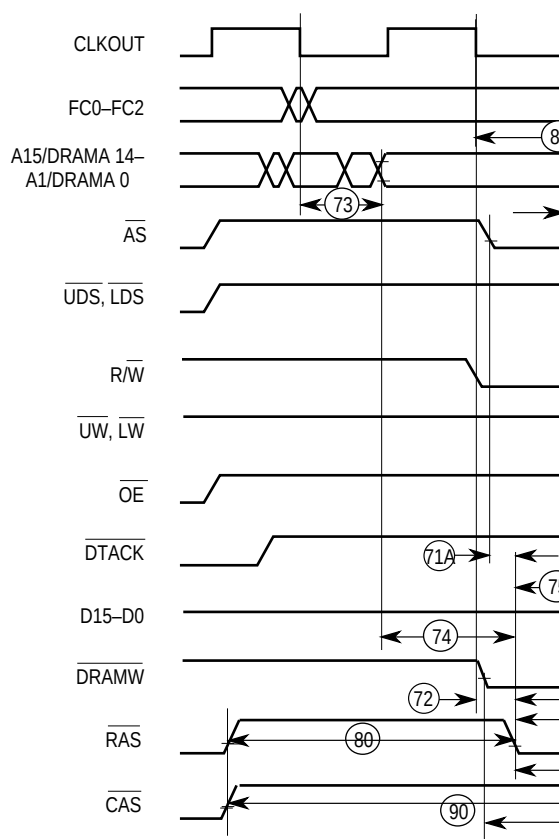


**Figure 8-5. Chip Select
Dia**



1-WAIT WRITE, NO REFRESH

Figure 8-9. DRAM Tir

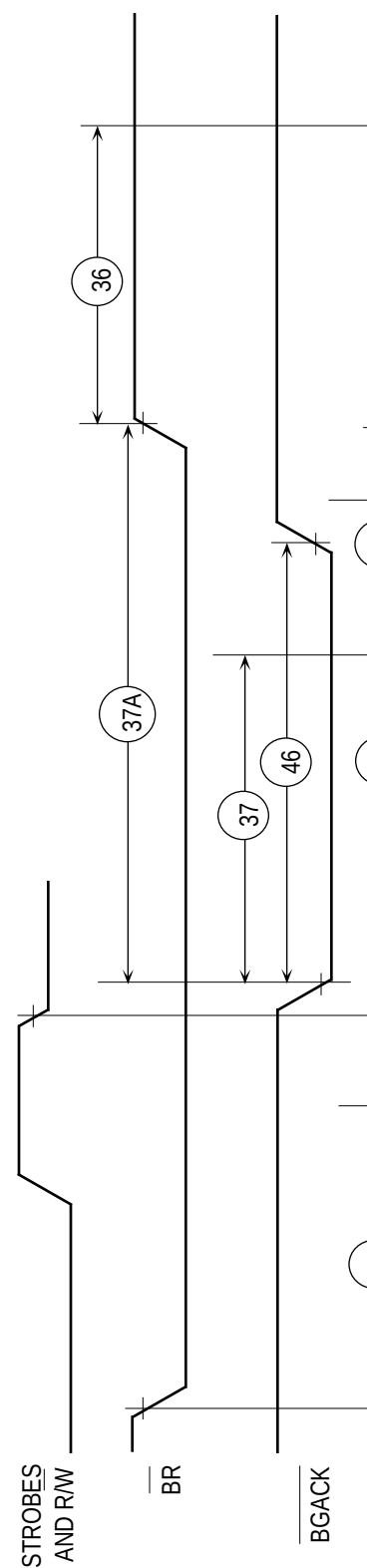


Figure 8-7. Bus

8.10 BUS OPERATION—DRAM ACCESS SPECIFICATIONS

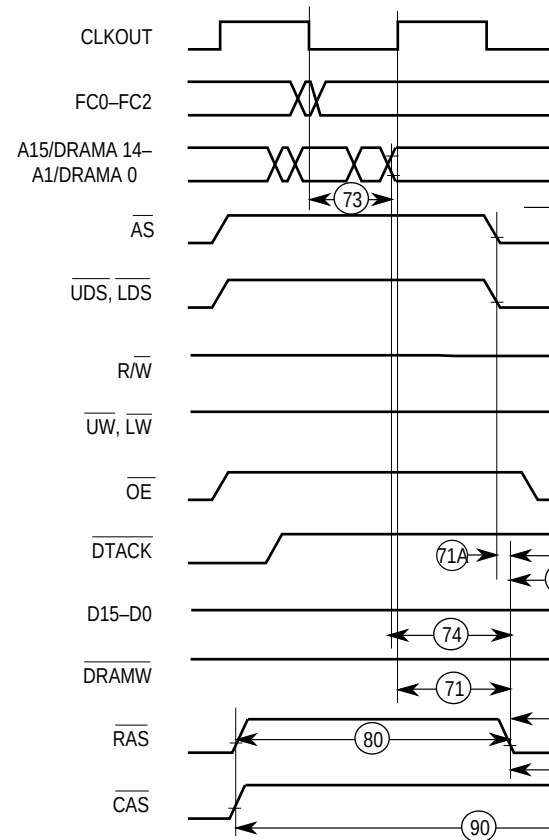
(The electrical specifications

8-8-8-11)

Num	Characteristic
71	CLKOUT High to RAS $\approx$ Asserted (0 Wait State Operation)
71A	AS Asserted to RAS $\approx$ Asserted (0 Wait State Operation)
72	CLKOUT Low to RAS $\approx$ Asserted (1 Wait State Operation)
73	CLKOUT Low to Row Address Valid
74	Row Address Valid to RAS $\approx$ Asserted
75	RAS $\approx$ Asserted to Row Address Invalid
76	CLKOUT High to Row Address Invalid (0 Wait State Operation)
77	CLKOUT Low to Row Address Invalid (1 Wait State Operation)
78	RAS $\approx$ Width Asserted (Non-Page Mode)
79	RAS $\approx$ Width Asserted (Page Mode)
80	RAS $\approx$ Width Negated (Back to Back Cycles)
81	RAS $\approx$ Asserted to CAS $\approx$ Asserted
82	CLKOUT High to Column Address Valid (0 Wait State Operation)
83	CLKOUT Low to Column Address Valid (1 Wait State Operation)
84	CLKOUT Low to CAS $\approx$ Asserted (0 Wait State Operation)
85	CLKOUT High to CAS $\approx$ Asserted (1 Wait State Operation)
86	Column Address Valid to CAS $\approx$ Asserted
87	CAS $\approx$ Asserted to Column Address Invalid
88	CAS $\approx$ Width Asserted
89	CLKOUT Low to RAS $\approx$ /CAS $\approx$ Negated
89A	AS Negated to RAS $\approx$ /CAS $\approx$ Negated
90	CAS $\approx$ Width Negated (Back to Back Cycles)
91	CAS $\approx$ Width Negated (Page Mode ²)
92	UDS/LDS Asserted to CAS $\approx$ Asserted ¹ (Page Mode)
93	DRAMW Low to CAS $\approx$ Asserted (Write)
94	Data Out Valid to CAS $\approx$ Asserted (Write)
95	CLKOUT Low to CAS $\approx$ Asserted (Refresh Cycle)
96	CLKOUT High to CAS $\approx$ Negated (Refresh Cycle)
97	CAS $\approx$ Width Asserted (Refresh Cycle)
98	CAS $\approx$ Asserted to RAS $\approx$ Asserted (Refresh Cycle)
99	CLKOUT High to RAS $\approx$ Asserted (Refresh Cycle)
100	CLKOUT Low to RAS $\approx$ Negated (Refresh Cycle)
101	RAS $\approx$ Width Asserted (Refresh Cycle)
102	DRAMW High to RAS $\approx$ Asserted (Refresh Cycle)
103	DRAMW High Hold After RAS $\approx$ Asserted (Refresh Cycle)

NOTES:

1. On write portion of TAS, CAS assertion is gated by operation).
2. Page mode is used on Read-Modify-Write (TAS ins



0-WAIT READ, NO REFRESH

Figure 8-8. DRAM Timing

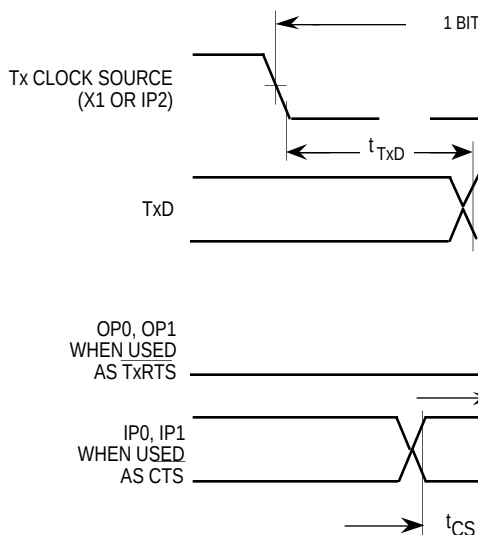


Figure 8-15

8.16 AC ELECTRICAL CHARACTER

(See Figure 8-16 and Note)

Characteristic
RxD Data Setup Time to RxC High
RxD Data Hold Time from RxC High
RTS Output Valid from Rx Clock

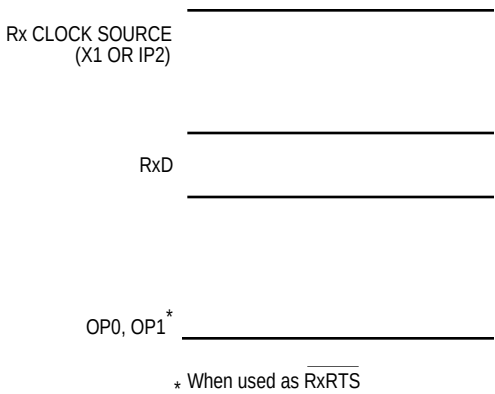
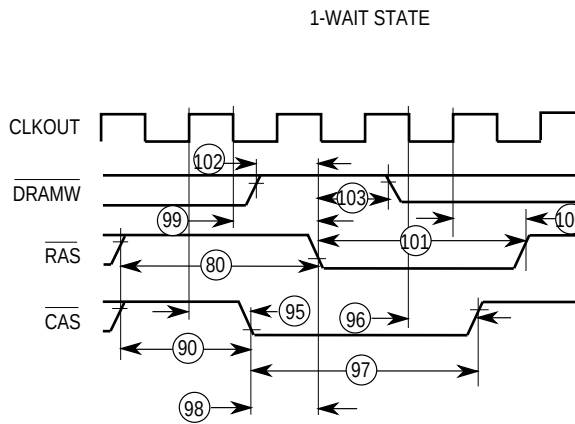
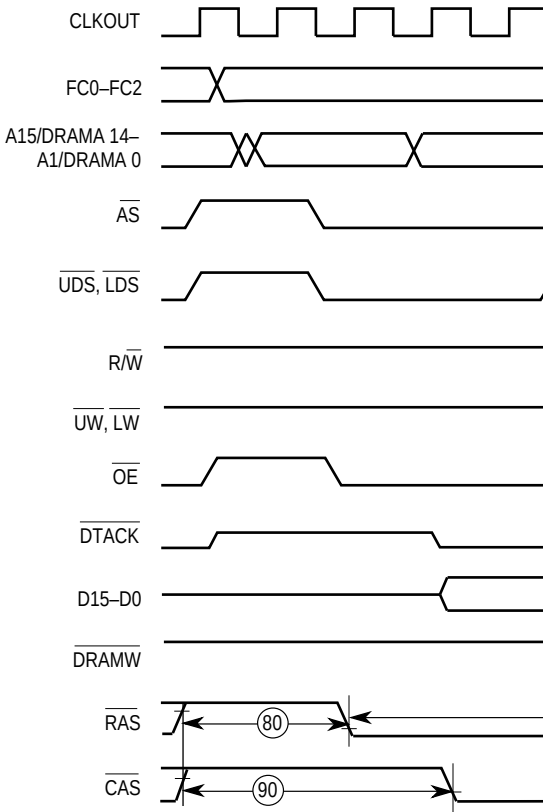


Figure 8-16



0 & 1-WAIT REFRE

Figure 8-10. DRAM



* NOTE: TAS IS A BYTE-ONLY INSTRUCTION, THEREFORE

Figure 8-11. DRAM

8.11 SERIAL MODULE ELECTRICAL

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 5\%$, See Note 1)

Characteristic
X1/CLK Input Leakage Current
X1/CLK Frequency (see Note 2)
Counter/Timer Clock Frequency (IP2)

NOTES:

1. All voltage measurements are referenced to ground (C_L = 150 pF, R_L = 750 Ω)

2. To use the standard baud rates selected by the clock-

frequency should be set to 3.6864 MHz or a 3.6864 M

3. IP5–2 for Rx, Tx are not supported in the MC68306

8.12 SERIAL MODULE AC ELECTRICAL CHARACTERISTICS

Characteristic
Counter/Timer Clock High or Low Time
Clock Rise Time
Clock Fall Time

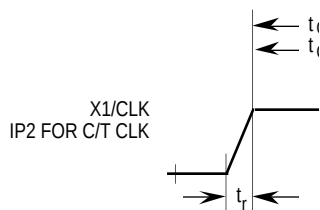


Figure 8-11

8.13 AC ELECTRICAL CHARACTERISTICS

(See Figure 8-13 and Note.)

Characteristic
Port Input Setup Time to LDS Asserted
Port Input Hold Time from LDS Negated
Port Output Valid from LDS Negated

NOTE: Test conditions for port outputs: $C_L = 50\text{ pF}$, $R_L = 2$

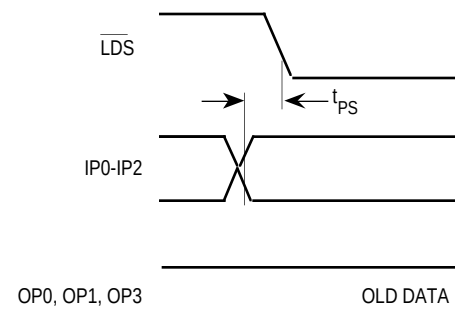
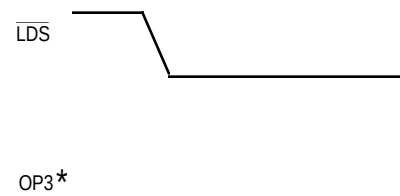


Figure 8-12

8.14 AC ELECTRICAL CHARACTERISTICS

Characteristic
OP3 High (When Used as Counter Interrupt) from LDS Negated

NOTE: Test conditions for interrupt output: $C_L = 50\text{ pF}$, $R_L = 2$



* When used as counter interrupt output.

Figure 8-14

8.15 AC ELECTRICAL CHARACTERISTICS

(See Figure 8-15 and Note)

Characteristic
TxD Output Valid from Tx Clock Low
CTS Input Setup to Tx Clock High *
CTS Input Hold from Tx Clock High *
RTS Output Valid from Tx Clock

* CTS is an asynchronous input. This specification is only for particular Tx clock edge.

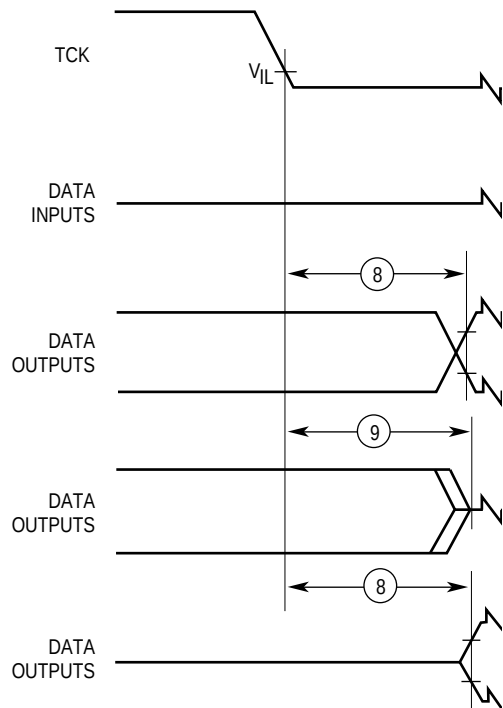


Figure 8-18. Bounce

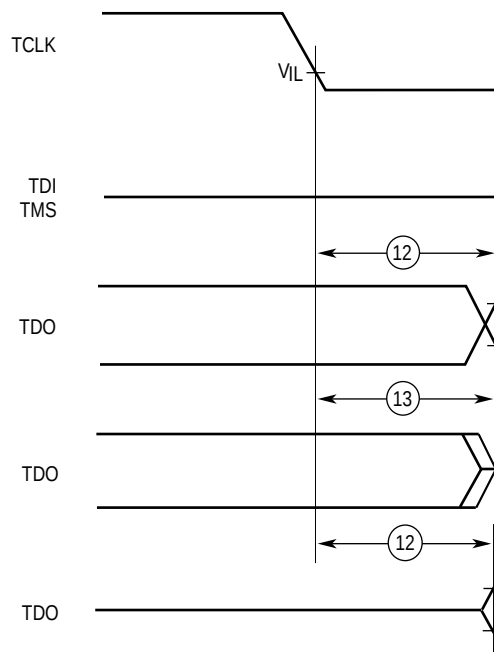


Figure 8-19. Test /

8.17 IEEE 1149.1 ELECTRICAL CH.

(The electrical specifications in this document are preliminary)

Num.	Characteristic
	TCK Frequency of Operation
1	TCK Cycle Time
2	TCK Clock Pulse Width Measured at 1.5 V
3	TCK Rise and Fall Times
6	Boundary Scan Input Data Setup Time
7	Boundary Scan Input Data Hold Time
8	TCK Low to Output Data Valid
9	TCK Low to Output High Impedance
10	TMS, TDI Data Setup Time
11	TMS, TDI Data Hold Time
12	TCK Low to TDO Data Valid
13	TCK Low to TDO High Impedance
14	TRST Width Low

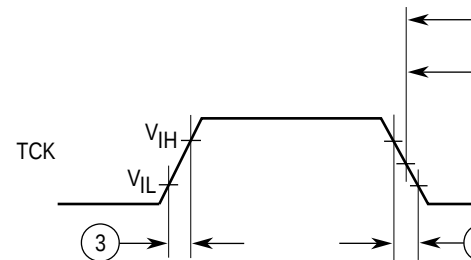


Figure 8-17. Test